

## **REMARKS**

### **Overview of the Office Action**

Claims 1-4, 12, 16, and 33 have been rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 6,291,839 ("Lester").

Claims 1, 14-15, 18-19, 30-31, and 34-35 have been rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 6,410,942 ("Thibeault").

Claims 18-20 and 37 have been rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 5,792,698 ("Nishitani").

Claims 5-11 and 13 have been rejected under 35 U.S.C. 103(a) as unpatentable over Lester.

Claim 17 has been rejected under 35 U.S.C. 103(a) as unpatentable over Lester in view of U.S. Patent No. 6,515,310 ("Yamazaki").

Claims 20-29 and 36 have been rejected under 35 U.S.C. 103(a) as unpatentable over Thibeault.

Claim 32 has been rejected under 35 U.S.C. 103(a) as unpatentable over Thibeault in view of Yamazaki.

### **Status of the claims**

Claim 1 has been amended.

Claims 1-37 remain pending.

Rejection of claims 1-4, 12, 16, and 33 under 35 U.S.C. §102(b)

The Office Action states that Lester teaches all of Applicants' recited elements.

Independent claim 1 recites, inter alia, a radiation-emitting semiconductor component that includes a multilayer structure "wherein... the semiconductor component is free of a deposition substrate of the multilayer structure", which Lester fails to teach or suggest.

Lester discloses a GaN-based LED that includes a hetero-junction device 10, having an emission layer 14 interposing an n-type layer 12 and a p-type layer 16, fabricated on a substrate 8 (i.e., deposition substrate). A reflector 9 is positioned on the backside of the substrate. An n-contact 18 is electrically connected to the n-type layer 12 while the p-contact 20 is electrically connected to the p-type layer 16. Both electrical contacts are preferably made from reflective metals (i.e., metals that reflect greater than 70% of normally incident visible light). A p-bond pad 21 is positioned on the p-contact (see col. 2, lines 57-67 and Fig. 1 of Lester).

The Examiner cites Fig. 5 of Lester as teaching Applicants' recited invention. Applicants disagree. As described above, and also as clearly shown in Fig. 5 of Lester, the multilayer device of Lester includes a substrate 8.

According to Lester "[t]he top surface of the LED has been roughened, preferably in alignment with the openings in the contact. This may be achieved by etching the GaN in a self-aligned fashion during the same lithographic step used to pattern the contact. The etched holes can extend into the p-layer 16 or can be etched as deep as the substrate" (see Fig. 5, and col. 5, lines 8-14 of Lester).

In contrast to Lester, and as clearly shown in Applicants' Fig. 1, Applicants' multilayer structure 12 is free of a deposition substrate. Therefore, Lester clearly fails to teach or suggest a radiation-emitting semiconductor component that includes a multilayer structure "wherein... the

semiconductor component is free of a deposition substrate of the multilayer structure”, as recited in Applicants’ amended claim 1.

In response to Applicants’ previous argument, the Examiner asserts that the term “semiconductor component” is merely a label and a broad limitation. The Examiner further asserts that the n type layer 12, the emission layer 14, and the p type layer 16 of Lester together can form Applicants’ recited semiconductor component without the substrate 8, and thus the multilayer structure of Lester is free of a deposition substrate. Applicants disagree with Examiner’s reasoning and interpretation of Lester.

The Examiner appears to argue that a “semiconductor component” is any arbitrary subsequence of single layers of a semiconductor chip. However, the Examiner’s assertion is far beyond any reasonable interpretation.

According to M.P.E.P. §2111,

“During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's *en banc* decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard: The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).”

According to Applicants’ specification, the recited semiconductor component refers to a completed device, and not some intermediate assembly of semiconductor layers. Further, one skilled in the art of semiconductors would know and understand that the term “semiconductor

component” refers to a completed device, such as a semiconductor chip and an associated optional package.

Additionally, one skilled in the art would evaluate the entirety of a cited reference to determine what the reference teaches. Consequently, one skilled in the art of semiconductors would know and understand that each of the references cited in the Office Action teaches a completed device, rather than an intermediate assembly of semiconductor layers

Applicants’ assertion is confirmed by Lester, itself, which states that the disclosed light emitting device (i.e., component) includes “an emission layer 14 interposing an n-type layer 12 and a p-type layer 16, fabricated on a substrate 8. A reflector 9 is positioned on the backside of the substrate” (see col. 2, lines 58-61 of Lester). The light emitting device of Fig. 5 of Lester further includes a p contact 20 and etched holes. There is no teaching or suggestion in Lester that the substrate 8 could be omitted, or that it is removed.

Clearly, the light emitting device disclosed by Lester does, in fact, include the substrate 8 (i.e., deposition substrate), and thus fails to teach or suggest Applicants’ recited semiconductor component, which “is free of a deposition substrate”.

Further, even if one skilled in the art were to remove the substrate from the device of Lester, the resulting device would not include a reflector as the Examiner asserts. The reflector 9 of Lester is disposed on the opposite side of the substrate. If the substrate is omitted or removed, then the reflector 9 must also necessarily be omitted or removed.

It is improper for the Examiner to hand pick particular ones of the multiple layers of the device of Lester, assemble those selected particular layers in an order contrary to the teachings of Lester, and then assert that such an artificial assembly anticipates Applicants’ recited invention.

Additionally, the Examiner points out that Applicants' Figures appear to show a substrate 30. Applicants fail to see the significance of the Examiner's point. The invention is defined by that which is recited in the claims, and not by specific embodiments that are disclosed in the specification. Further, the substrate 30 shown in Applicants' figures is a carrier substrate, to which the Applicants' recited semiconductor component is affixed. Applicants' claims recite that the semiconductor component "is free of a deposition substrate". It is well known in the art that a carrier substrate is not the same as a deposition substrate (which is explicitly disclosed by Lester and the other cited references discussed below).

In view of the foregoing, Applicants submit that Lester fails to teach or suggest the subject matter recited in independent claim 1. Accordingly, claim 1 is patentable over Lester under 35 U.S.C. §102(b).

#### Dependent claims

Claims 1-4, 12, 16, and 33, which depend from independent claim 1, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Lester for at least those reasons discussed above with respect to claim 1.

#### Rejection of claims 1, 14-15, 18-19, 30-31, and 34-35 under 35 U.S.C. §102(b)

The Office Action states that Thibeault teaches all of Applicants' recited elements.

As discussed above, independent claim 1 recites, inter alia, a radiation-emitting semiconductor component that includes a multilayer structure "wherein... the semiconductor component is free of a deposition substrate of the multilayer structure", which Thibeault fails to teach or suggest.

Thibeault discloses an LED 30 utilizing a flip-chip mounting. Micro-LEDs 32 are formed in an array by etching away semiconductor material of a full LED structure. Each micro-LED 32 has an active layer surrounded by two oppositely doped layers. Each of the micro-LEDs 32 has angled side surfaces and a top layer that is narrower than a bottom layer. The micro-LED array is formed on a first spreader layer 34 that is formed on a substrate 36 (i.e., a deposition substrate). An insulating layer 38 covers the micro-LEDs and the surface of the first spreader between adjacent micro-LEDs. On each micro-LED 32, a hole is included in the insulating layer 38 for a top contact 40. A second spreader layer 42 coats the entire micro-LED array to interconnect the top contacts 40 (see Fig. 3, and col. 6, line 53 to col. 7, line 2 of Thibeault).

The Examiner cites Fig. 3 of Thibeault as teaching Applicants' recited invention. Applicants respectfully disagree. As described above, and also as clearly shown in Fig. 3 of Thibeault, the multilayer device of Thibeault includes a substrate 36.

In contrast to Thibeault, and as clearly shown in Applicants' Fig. 5, Applicants' multilayer structure 12 is free of a deposition substrate. Therefore, Thibeault clearly fails to teach or suggest a radiation-emitting semiconductor component that includes a multilayer structure "wherein... the semiconductor component is free of a deposition substrate of the multilayer structure", as recited in Applicants' claim 1.

In response to Applicants' previous argument, the Examiner again asserts that the term "semiconductor component" is merely a label and a broad limitation. The Examiner further asserts that the n type layer, the emission layer 32, the p type layer, and the reflective layer 48 of Thibeault together can form Applicants' recited multilayer structure without the substrate 36, and thus the multilayer structure of Thibeault is free of a deposition substrate. Applicants disagree with the Examiner's reasoning and interpretation of Thibeault.

The Examiner again appears to argue that a “semiconductor component” is any arbitrary subsequence of single layers of a semiconductor chip. However, here too the Examiner’s assertion is far beyond any reasonable interpretation.

Applicants again refer the Examiner to M.P.E.P. §2111, and maintain that one skilled in the art of semiconductors knows and understands that the term “semiconductor component” refers to a completed device, such as a semiconductor chip and associated package.

Applicants’ assertion is again confirmed by Thibeault, which states that the light emitting device 30 (i.e., semiconductor component) includes a substrate 36. There is no teaching or suggestion in Thibeault that the substrate 36 could be omitted, or is removed, in defining or delineating the semiconductor component.

Clearly, the light emitting device 30 disclosed by Thibeault does, in fact, include the substrate 36, the person of skill would view and understand it that way, and it thus fails to teach or suggest Applicants’ recited semiconductor component, which “is free of a deposition substrate”. Indeed, the Thibeault teaching is quite to the contrary of Applicants’ claimed component.

Independent 18 recites limitations similar to those of independent claim 1 and is, therefore, deemed to be patentably distinct over Thibeault for at least those reasons discussed above with respect to claim 1.

In view of the foregoing, Applicants submit that Thibeault fails to teach or suggest the subject matter recited in independent claims 1 and 18. Accordingly, claims 1 and 18 are patentable over Thibeault under 35 U.S.C. §102(b).

### Dependent claims

Claims 14-15, 19, 30-31, and 34-35, which depend from independent claims 1 and 18, incorporate all of the limitations of the corresponding independent claim and are, therefore, deemed to be patentably distinct over Thibeault for at least those reasons discussed above with respect to claims 1 and 18.

### Rejection of claims 18-20 and 37 under 35 U.S.C. §102(b)

The Office Action states that Nishitani teaches all of Applicants' recited elements.

Independent claim 18 recites, inter alia, a radiation-emitting semiconductor component that includes a multilayer structure "wherein... the semiconductor component is free of a deposition substrate of the multilayer structure", which Lester fails to teach or suggest.

Nishitani discloses a semiconductor light emitting device (i.e., a semiconductor component). The semiconductor light emitting device includes an n-GaAs substrate 1 (i.e., deposition substrate) on which an n-GaAs buffer layer 2, an n-InAlP/GaAs light reflection layer 3, an n-InGaAlP clad layer 4, an undoped InGaAlP active layer 5, a p-InGaAlP clad layer 6, a p-GaAlAs current diffusion layer 7, and a p-GaAlAs light scattering layer 8 are sequentially deposited. A metal electrode 9 is formed at the center on the top face of the light scattering layer 8, and a metal electrode 10 is formed over the bottom face of the substrate 1. The light reflection layer 3 has a multilayer structure consisting of n-InAlP and n-GaAs layers that are alternately laid one atop another (see col. 3, lines 9-24 of Nishitani).

In contrast to Nishitani, and as clearly shown in Applicants' Fig. 5, Applicants' multilayer structure 12 is free of a deposition substrate. Therefore, Nishitani clearly fails to teach or suggest a radiation-emitting semiconductor component that includes a multilayer



structure “wherein... the semiconductor component is free of a deposition substrate of the multilayer structure”, as recited in Applicants’ claim 1.

The Examiner cites Fig. 4 of Nishitani as allegedly teaching Applicants’ recited invention. Here, again, the Examiner asserts that the term “semiconductor component” is merely a label and a broad limitation. The Examiner further asserts that the n type layer 4, the emission layer 5, the p type layer 6, and the reflective layer 9 of Nishitani together can form Applicants’ recited semiconductor component without the substrate 1, and thus that the multilayer structure of Thibeault is free of a deposition substrate. Applicants disagree with the Examiner’s reasoning and interpretation of Nishitani.

The Examiner yet again appears to argue that a “semiconductor component” is any arbitrary subsequence of single layers of a semiconductor chip. However, the Examiner’s assertion remains far beyond any reasonable interpretation.

Applicants again refer the Examiner to M.P.E.P. §2111, and maintain that one skilled in the art of semiconductors knows and understands that the term “semiconductor component” refers to a completed device, such as a semiconductor chip and an optional package.

Applicants’ assertion is (as discussed above) confirmed by Nishitani, which states and teaches that the light emitting device 30 (i.e., the semiconductor component) includes a substrate 1. There is no teaching or suggestion in Nishitani that the substrate 1 could be omitted, or is removed.

Clearly, the light emitting device disclosed by Nishitani does, in fact, and is understood by the person of skill to include the substrate 1, and thus fails to teach or suggest Applicants’ recited semiconductor component, which “is free of a deposition substrate”.

In view of the foregoing, Applicants submit that Nishitani fails to teach or suggest the subject matter recited in independent claim 18. Accordingly, claim 18 is patentable over Nishitani under 35 U.S.C. §102(b).

#### Dependent claims

Claims 19-20 and 37, which depend from independent claim 18, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Nishitani for at least those reasons discussed above with respect to claim 18.

#### Rejection of claims 5-11 and 13 under 35 U.S.C. §103(a)

The Office Action states that Lester teaches all of Applicants' elements recited in claim 1.

As previously discussed, Lester fails to teach or suggest the subject matter recited in Applicants' independent claim 1.

Claims 5-11 and 13, which depend from independent claim 1, incorporate all of the limitations of independent claim 1 and are, therefore, deemed to be patentably distinct over Lester for at least those reasons discussed above with respect to independent claim 1.

#### Rejection of claims 17 under 35 U.S.C. 103(a)

The Office Action states that the combination of Lester and Yamazaki teaches all of Applicants' recited elements.

As previously discussed, Lester fails to teach or suggest the subject matter recited in Applicant's independent claim 1.

Because Lester fails to teach or suggest the subject matter recited in amended claim 1, and because Yamazaki fails to teach or suggest the elements of claim 1 that Lester is missing, the addition of Yamazaki to the Lester reference fails to remedy the above-described deficiencies of Lester.

Claim 17, which depends from independent claim 1, incorporates all of the limitations of independent claim 1 and is, therefore, deemed to be patentably distinct over Lester and Yamazaki for at least those reasons discussed above with respect to independent claim 1.

Rejection of claims 20-29 and 36 under 35 U.S.C. 103(a)

The Office Action states that Thibeault teaches all of Applicants' elements recited in claim 18.

As previously discussed, Thibeault fails to teach or suggest the subject matter recited in Applicants' independent claim 18.

Claims 20-29 and 36, which depend from amended independent claim 18, incorporate all of the limitations of independent claim 18 and are, therefore, deemed to be patentably distinct over Thibeault for at least those reasons discussed above with respect to claim 18.

Rejection of claim 32 under 35 U.S.C. 103(a)

The Office Action states that the combination of Thibeault and Yamazaki teaches all of Applicants' recited elements.

As previously discussed, Thibeault fails to teach or suggest the subject matter recited in Applicant's independent claim 18.

Because Thibeault fails to teach or suggest the subject matter recited in amended claim 18, and because Yamazaki fails to teach or suggest the elements of claim 18 that Thibeault is missing, the addition of Yamazaki to the Thibeault reference fails to remedy the above-described deficiencies of Thibeault.

Claim 32, which depends from independent claim 18, incorporates all of the limitations of independent claim 18 and is, therefore, deemed to be patentably distinct over Thibeault and Yamazaki for at least those reasons discussed above with respect to independent claim 18.

#### Conclusion

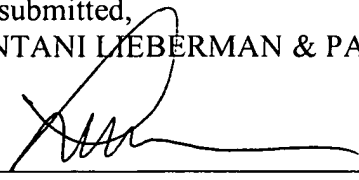
In view of the foregoing, reconsideration and withdrawal of all rejections, and allowance of all pending claims, are respectfully solicited.

Should the Examiner have any comments, questions, suggestions, or objections, the Examiner is respectfully requested to telephone the undersigned to facilitate an early resolution of any outstanding issues.

It is believed that no fees or charges are required at this time in connection with the present application. However, if any fees or charges are required at this time, they may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,  
COHEN PONTANI LIEBERMAN & PAVANE LLP

By



Lance J. Lieberman  
Reg. No. 28,437  
551 Fifth Avenue, Suite 1210  
New York, New York 10176  
(212) 687-2770

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